





PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Katsuji KIMURA

Appln. No.: 09/940,472

Confirmation No.: 4891

Filed: August 29, 2001

For: LINEAR VOLTAGE SUBTRACTOR/ADDER

CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

RESPONSE TO RESTRICTION REQUIREMENT

TECHNOLOGY CENTER, 2800

APR 23 2002

Commissioner for Patents Washington, D.C. 20231

Sir:

In response to the Office Action dated March 26, 2002 in which the Examiner has required a restriction, Applicant responds by electing Group I, *i.e.*, claims 1-4, drawn to voltage subtractor/adder circuits, classified in class 327, subclass 361. This election is made without prejudice to the filing of a divisional application directed to claims 5-13.

Prompt and favorable action on the elected claims is now respectfully requested.

Respectfully submitted,

Group Art Unit: 2816

Examiner: Minh T. NGUYEN

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Date: April 22, 2002

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